# 1 MHz Bandwidth Low Power Op Amp

## Features

- Available in SC-70-5 and SOT-23-5 packages
- 1 MHz Gain Bandwidth Product (typ.)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 5.5V
- Supply Current: $I_Q$ = 100 µA (typ.)
- 90° Phase Margin (typ.)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

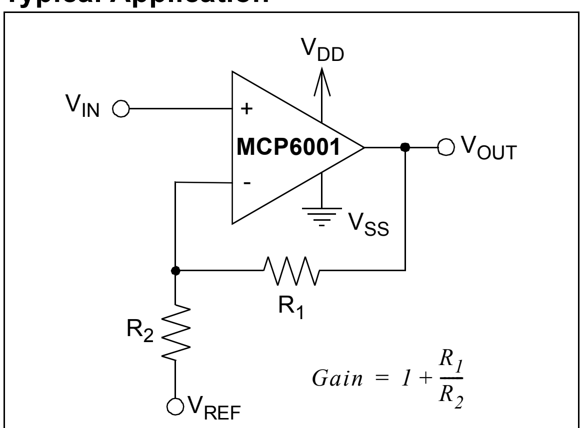
## Applications

- Automotive
- Portable Equipment
- Photodiode Pre-amps
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

## Available Tools

Spice Macro Models (at www.microchip.com)
FilterLab® Software (at www.microchip.com)

## Typical Application



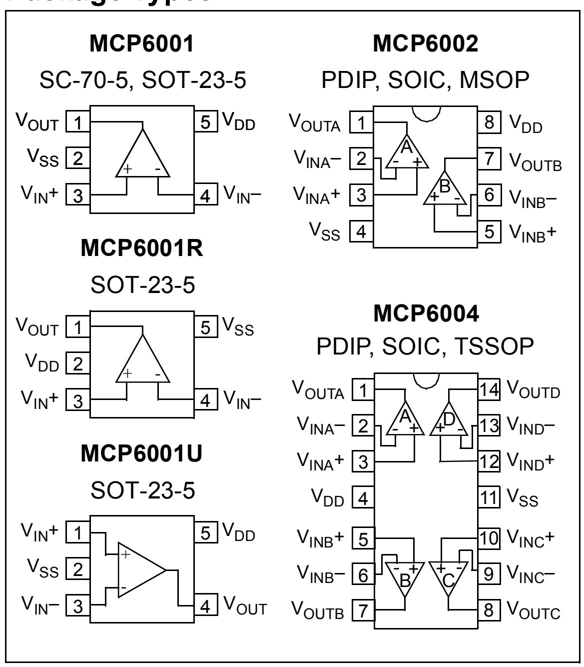

**Non-Inverting Amplifier**

## Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz gain bandwidth product and 90° phase margin (typ.). It also maintains 45° phase margin (typ.) with 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 µA (typ.) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of $V_{DD}$ + 300 mV to $V_{SS}$ - 300 mV. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges. It also has a power supply range of 1.8V to 5.5V.

## Package Types



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD}$ - $V_{SS}$ ........................................................................7.0V
All Inputs and Outputs ..................... $V_{SS}$ -0.3V to $V_{DD}$ +0.3V
Difference Input Voltage ...................................... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .................................continuous
Current at Input Pins ....................................................±2 mA
Current at Output and Supply Pins ...........................±30 mA
Storage Temperature ...................................-65°C to +150°C
Maximum Junction Temperature ($T_J$) .......................... +150°C
ESD Protection On All Pins (HBM;MM) .............. ≥ 4 kV; 200V

**† Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

| Name | Function |
|---|---|
| $V_{IN}+$, $V_{INA}+$, $V_{INB}+$, $V_{INC}+$, $V_{IND}+$ | Non-inverting Inputs |
| $V_{IN}-$, $V_{INA}-$, $V_{INB}-$, $V_{INC}-$, $V_{IND}-$ | Inverting Inputs |
| $V_{DD}$ | Positive Power Supply |
| $V_{SS}$ | Negative Power Supply |
| $V_{OUT}$, $V_{OUTA}$, $V_{OUTB}$, $V_{OUTC}$, $V_{OUTD}$ | Outputs |

## DC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics**: Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +1.8V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}/2$, $R_L$ = 10 kΩ to $V_{DD}/2$, and $V_{OUT} \sim V_{DD}/2$.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | -7.0 | — | +7.0 | mV | $V_{CM} = V_{SS}$ |
| Input Offset Drift with Temperature | $\Delta V_{OS}/\Delta T_A$ | — | ±2.0 | — | µV/°C | $T_A$= -40°C to +125°C, $V_{CM} = V_{SS}$ |
| Power Supply Rejection | PSRR | — | 86 | — | dB | $V_{CM} = V_{SS}$ |
| **Input Bias Current and Impedance** | | | | | | |
| Input Bias Current: | $I_B$ | — | ±1.0 | — | pA | |
| Industrial Temperature | $I_B$ | — | 19 | — | pA | $T_A$ = +85°C |
| Extended Temperature | $I_B$ | — | 1100 | — | pA | $T_A$ = +125°C |
| Input Offset Current | $I_{OS}$ | — | ±1.0 | — | pA | |
| Common Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$‖6 | — | Ω‖pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$‖3 | — | Ω‖pF | |
| Common Mode | | | | | | |
| Common Mode Input Range | $V_{CMR}$ | $V_{SS} - 0.3$ | — | $V_{DD} + 0.3$ | V | |
| Common Mode Rejection Ratio | CMRR | 60 | 76 | — | dB | $V_{CM}$ = -0.3V to 5.3V, $V_{DD}$ = 5V |
| **Open-Loop Gain** | | | | | | |
| DC Open-Loop Gain (large signal) | $A_{OL}$ | 88 | 112 | — | dB | $V_{OUT}$ = 0.3V to $V_{DD}$ - 0.3V, $V_{CM} = V_{SS}$ |
| **Output** | | | | | | |
| Maximum Output Voltage Swing | $V_{OL}$, $V_{OH}$ | $V_{SS}$ + 25 | — | $V_{DD}$ – 25 | mV | $V_{DD}$ = 5.5V |
| Output Short-Circuit Current | $I_{SC}$ | — | ±6 | — | mA | $V_{DD}$ = 1.8V |
| | | — | ±23 | — | mA | $V_{DD}$ = 5.5V |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 1.8 | — | 5.5 | V | |
| Quiescent Current per Amplifier | $I_Q$ | 50 | 100 | 170 | µA | $I_O$ = 0, $V_{DD}$ = 5.5V, $V_{CM}$ = 5V |

## AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +1.8 to 5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT} \approx V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, and $C_L$ = 60 pF.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **AC Response** | | | | | | |
| Gain Bandwidth Product | GBWP | — | 1.0 | — | MHz | |
| Phase Margin | PM | — | 90 | — | ° | G = +1 |
| Slew Rate | SR | — | 0.6 | — | V/µs | |
| **Noise** | | | | | | |
| Input Noise Voltage | $E_{ni}$ | — | 6.1 | — | µVp-p | f = 0.1 Hz to 10 Hz |
| Input Noise Voltage Density | $e_{ni}$ | — | 28 | — | nV/√Hz | f = 1 kHz |
| Input Noise Current Density | $i_{ni}$ | — | 0.6 | — | fA/√Hz | f = 1 kHz |

## TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $V_{DD}$ = +1.8V to +5.5V, and $V_{SS}$ = GND.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Industrial Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Extended Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **(Note)** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 5L-SC70 | $\theta_{JA}$ | — | 331 | — | °C/W | |
| Thermal Resistance, 5L-SOT-23 | $\theta_{JA}$ | — | 256 | — | °C/W | |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 85 | — | °C/W | |
| Thermal Resistance, 8L-SOIC (150 mil) | $\theta_{JA}$ | — | 163 | — | °C/W | |
| Thermal Resistance, 8L-SOIC (208 mil) | $\theta_{JA}$ | — | 118 | — | °C/W | |
| Thermal Resistance, 8L-MSOP | $\theta_{JA}$ | — | 206 | — | °C/W | |
| Thermal Resistance, 14L-PDIP | $\theta_{JA}$ | — | 70 | — | °C/W | |
| Thermal Resistance, 14L-SOIC | $\theta_{JA}$ | — | 120 | — | °C/W | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |

**Note:** The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature ($T_J$) must not exceed the Absolute Maximum specification of +150°C.

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +1.8V to +5.5V, $V_{SS}$ = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L$ = 10 kΩ to $V_{DD}/2$, and $C_L$ = 60 pF.

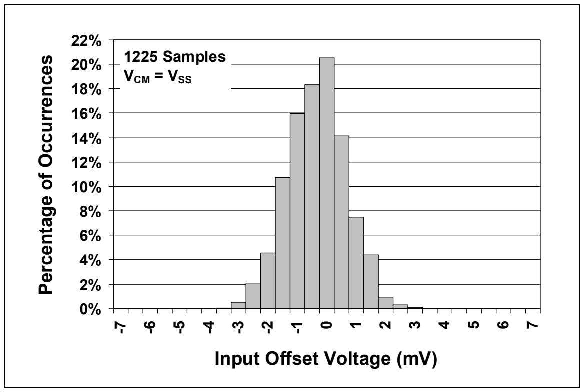



***FIGURE 2-1:*** *Input Offset Voltage Histogram.*

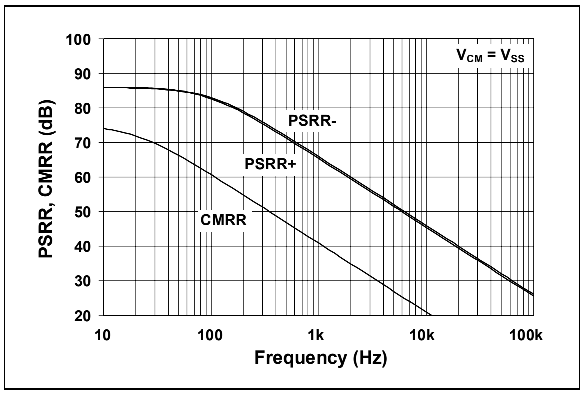



***FIGURE 2-2:*** *PSRR, CMRR vs. Frequency.*

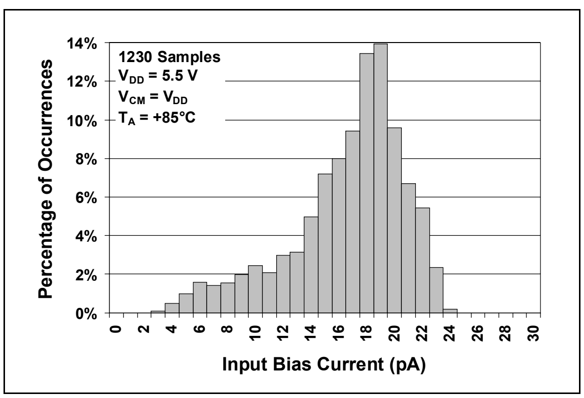



***FIGURE 2-3:*** *Input Bias Current at +85°C Histogram.*

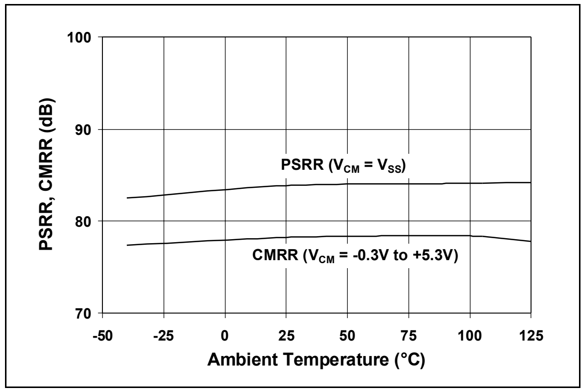



***FIGURE 2-4:*** *CMRR, PSRR vs. Ambient Temperature.*

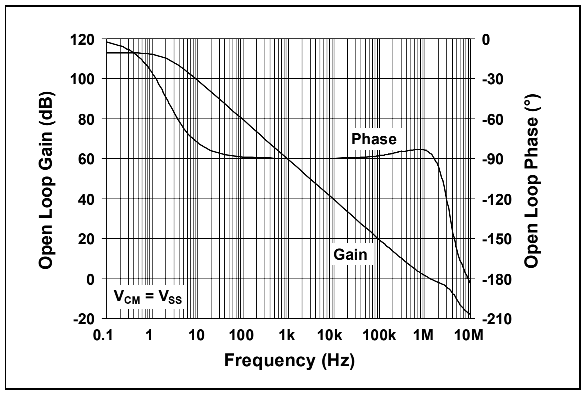



***FIGURE 2-5:*** *Open-Loop Gain, Phase vs. Frequency.*

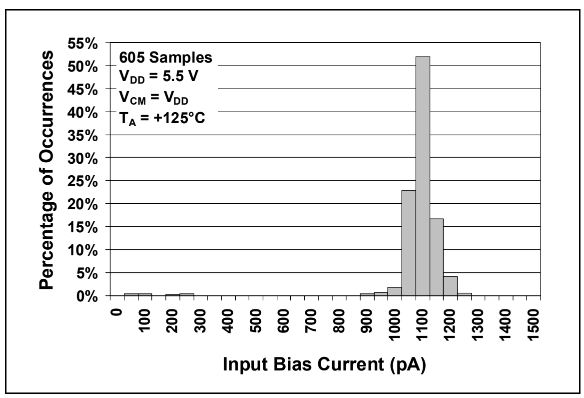



***FIGURE 2-6:*** *Input Bias Current at +125°C Histogram.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +1.8V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT} \approx V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, and $C_L$ = 60 pF.

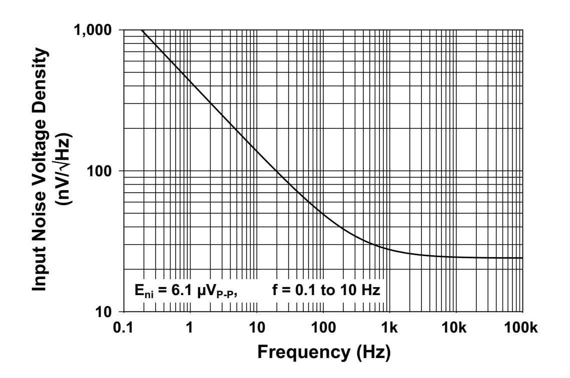



*FIGURE 2-7: Input Noise Voltage Density vs. Frequency.*

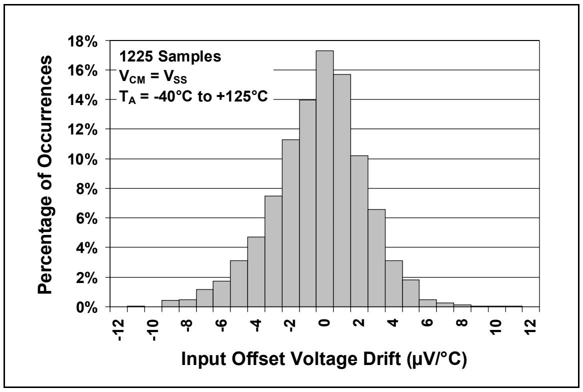



*FIGURE 2-10: Input Offset Voltage Drift Histogram.*

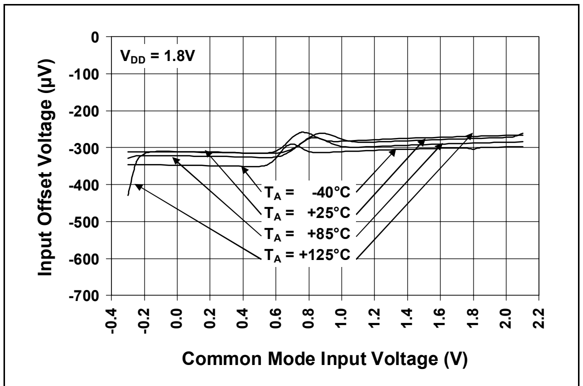



*FIGURE 2-8: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD}$ = 1.8V.*

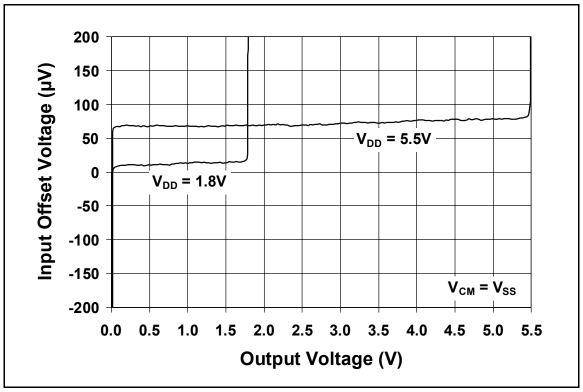



*FIGURE 2-11: Input Offset Voltage vs. Output Voltage.*

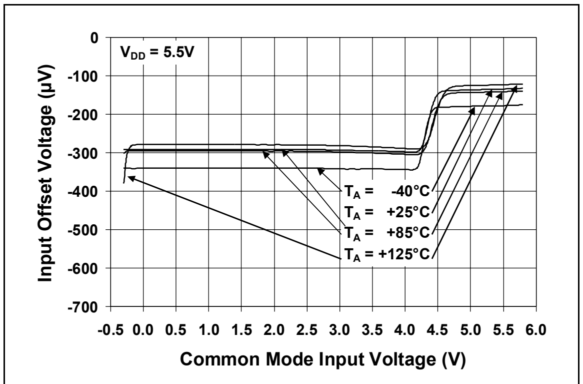



*FIGURE 2-9: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD}$ = 5.5V.*

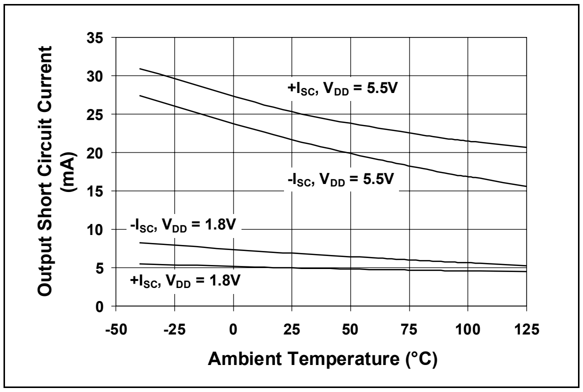



*FIGURE 2-12: Output Short-Circuit Current vs. Ambient Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C, $V_{DD}$ = +1.8V to +5.5V, $V_{SS}$ = GND, $V_{CM}$ = $V_{DD}$/2, $V_{OUT} \approx V_{DD}$/2, $R_L$ = 10 kΩ to $V_{DD}$/2, and $C_L$ = 60 pF.

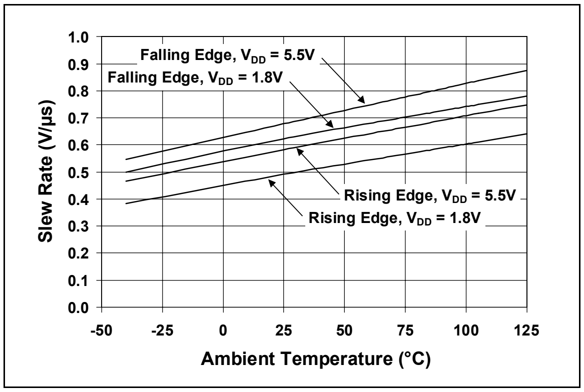



***FIGURE 2-13:*** *Slew Rate vs. Ambient Temperature.*

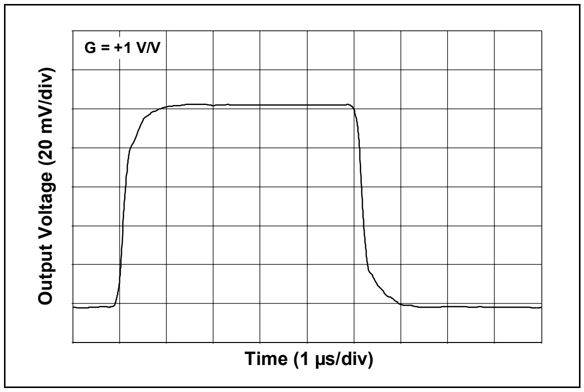



***FIGURE 2-16:*** *Small Signal Non-Inverting Pulse Response.*

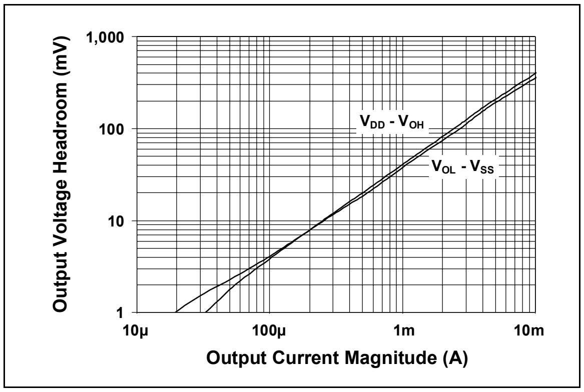



***FIGURE 2-14:*** *Output Voltage Headroom vs. Output Current Magnitude.*

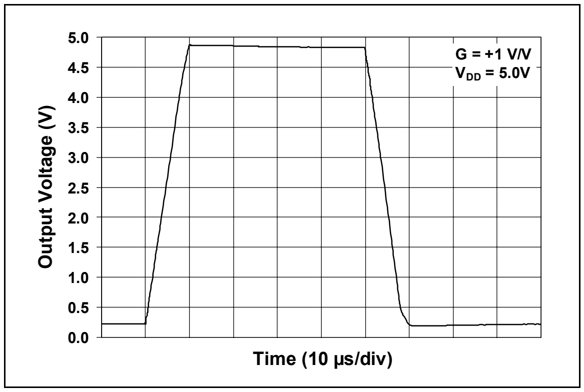



***FIGURE 2-17:*** *Large Signal Non-Inverting Pulse Response.*

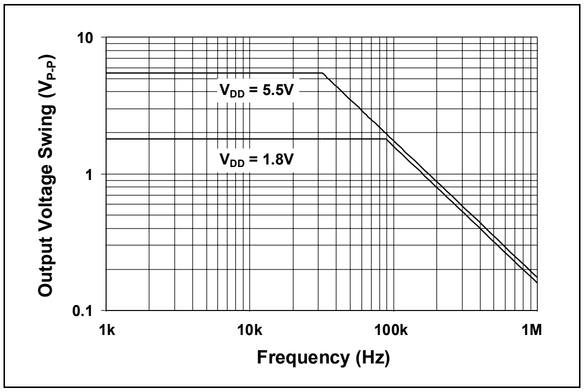



***FIGURE 2-15:*** *Output Voltage Swing vs. Frequency.*

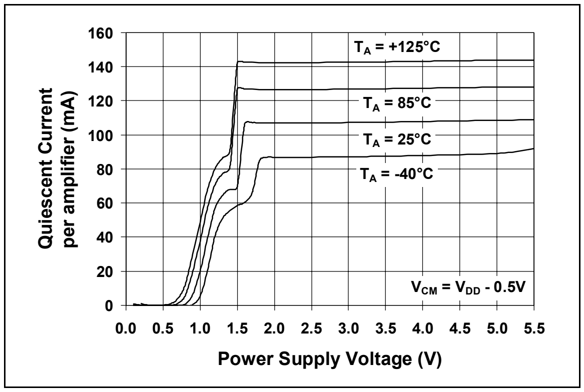



***FIGURE 2-18:*** *Quiescent Current vs. Power Supply Voltage.*

## 3.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low cost, low power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

### 3.1 Rail-to-Rail Input

The MCP6001/2/4 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows the input voltage exceeding the supply voltage without any phase reversal.

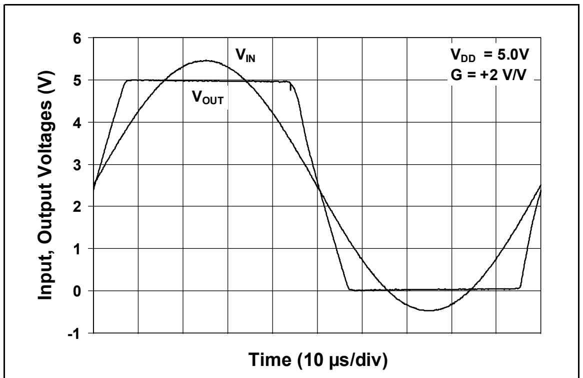
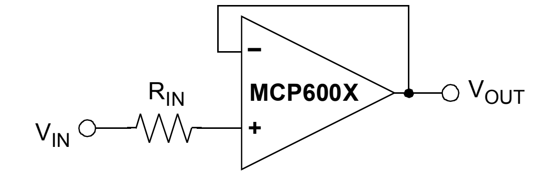



***FIGURE 3-1:*** *The MCP6001/2/4 Shows No Phase Reversal.*

The input stage of the MCP6001/2/4 op amp uses two differential input stages in parallel; one operates at low common mode input voltage ($V_{CM}$) and the other at high $V_{CM}$. With this topology, the device operates with $V_{CM}$ up to 300 mV above $V_{DD}$ and 300 mV below $V_{SS}$. The Input Offset Voltage is measured at $V_{CM} = V_{SS}$ - 300 mV and $V_{DD}$ + 300 mV to ensure proper operation.

Input voltages that exceed the input voltage range ($V_{SS}$ - 0.3V to $V_{DD}$ + 0.3V at 25°C) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 3-2.




$$R_{IN} \geq \frac{(Maximum\ expected\ V_{IN}) - V_{DD}}{2\ mA}$$

$$R_{IN} \geq \frac{V_{SS} - (Minimum\ expected\ V_{IN})}{2\ mA}$$

***FIGURE 3-2:*** *Input Current Limiting Resistor ($R_{IN}$).*

### 3.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amp is $V_{DD}$ - 25 mV (min.) and $V_{SS}$ + 25 mV (max.) when $R_L$ = 10 kΩ is connected to $V_{DD}/2$ and $V_{DD}$ = 5.5V. Refer to Figure 2-14 for more information.

### 3.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity gain buffer (G = +1) is the most sensitive to capacitive loads, but all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output ($R_{ISO}$ in Figure 3-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. It does not, however, improve the bandwidth.

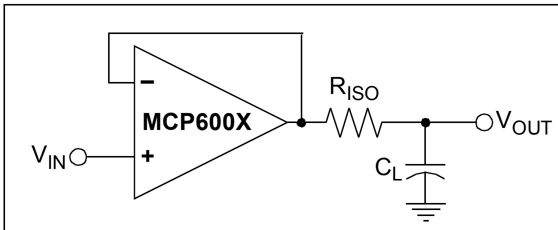



***FIGURE 3-3:*** *Output resistor, $R_{ISO}$ stabilizes large capacitive loads.*

To select $R_{ISO}$, check the frequency response peaking (or step response overshoot) on the bench (or with the MCP6001/2/4 Spice macro model). If the response is reasonable, you do not need $R_{ISO}$. Otherwise, start $R_{ISO}$ at 1 kΩ and modify its value until the response is reasonable.

## 3.4 Supply Bypass

With this family of operation amplifiers, the power supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other parts.

## 3.5 PCB Surface Leakage

In applications where low input bias current is critical, PCB (printed circuit board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA, if current-to-flow; this is greater than the MCP6001/2/4 family's bias current at 25°C (1 pA, typ).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-4.

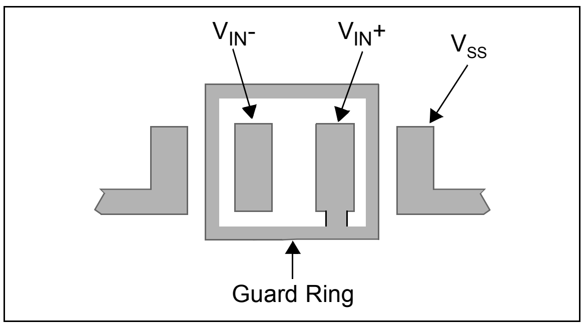



***FIGURE 3-4:*** *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a. Connect the non-inverting pin ($V_{IN}$+) to the input with a wire that does not touch the pcb surface.
   b. Connect the guard ring to the inverting input pin ($V_{IN}$–). This biases the guard ring to the common mode input voltage.
2. Inverting and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}$+). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin ($V_{IN}$–) to the input with a wire that does not touch the PCB surface.

## 3.6 Application Circuits

### 3.6.1 UNITY GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 3-5.

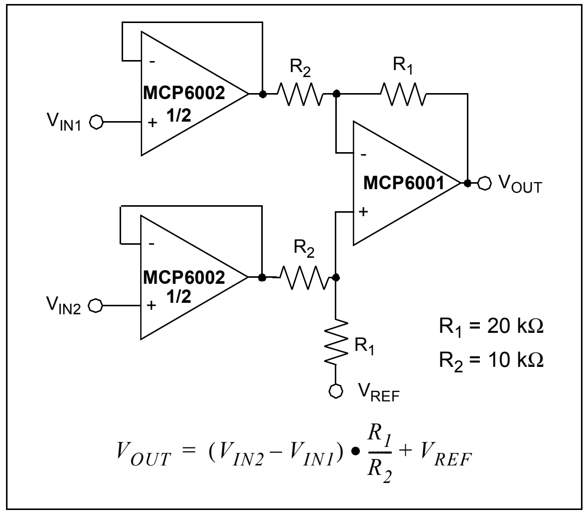



***FIGURE 3-5:*** *Instrumentation Amplifier with Unity Gain Buffer Inputs.*

### 3.6.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

It is possible to have a filter cutoff frequency as high as 1/10th of the op amp bandwidth (100 kHz). Figure 3-6 shows a second-order butterworth filter with 100 kHz cutoff frequency and a gain of +1V/V.

The component values were selected using Microchip's FilterLab® software.

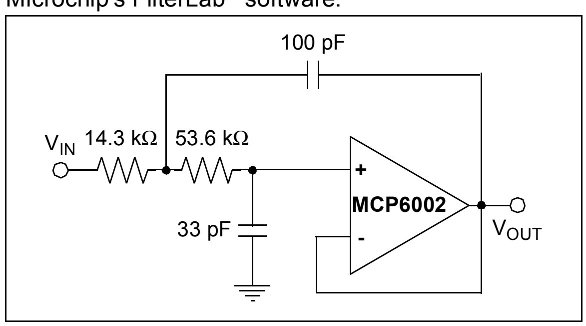



***FIGURE 3-6:*** *Active Second-Order Low-Pass Filter.*

### 3.6.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input and output and low input bias current, which makes this device suitable for a peak detector applications. Figure 3-7 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 3-7.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on $C_1$ is sampled to $C_2$ for a sample time defined by $t_{SAMP}$. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, $C_1$ discharges through $R_1$ for a time defined by $t_{CLEAR}$. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of $V_{IN}$ on $C_1$ for a time defined by $t_{DETECT}$.

In order to define the $t_{SAMP}$ and $t_{CLEAR}$, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time ($\tau$) is defined using $R_1$ ($\tau = R_1 {*} C_1$). $t_{DETECT}$ is the time that the input signal is sampled on $C_1$, and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both $C_1$ and $C_2$), could create slewing limitations as the input voltage ($V_{IN}$) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with op amp short-circuit current of $I_{SC}$ = 25 mA and load capacitor of $C_1$ = 0.1 µF, then:

**EQUATION**

$$I_{SC} = C_1 \times \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25mA}{0.1\mu F}$$

$$\frac{dV_{C1}}{dt} = \frac{250mV}{\mu s}$$

This voltage change rate is less than the MCP6001/2/4 slew rate of 600 mV/µs. When the input voltage swings below the voltage across $C_1$, $D_1$ becomes reverse-biased, which opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 µF and a stabilizing resistor ($R_{ISO}$) needs to be properly selected. Refer to Section 3.3, “Capacitive Load and Stability”, for op amp stability.

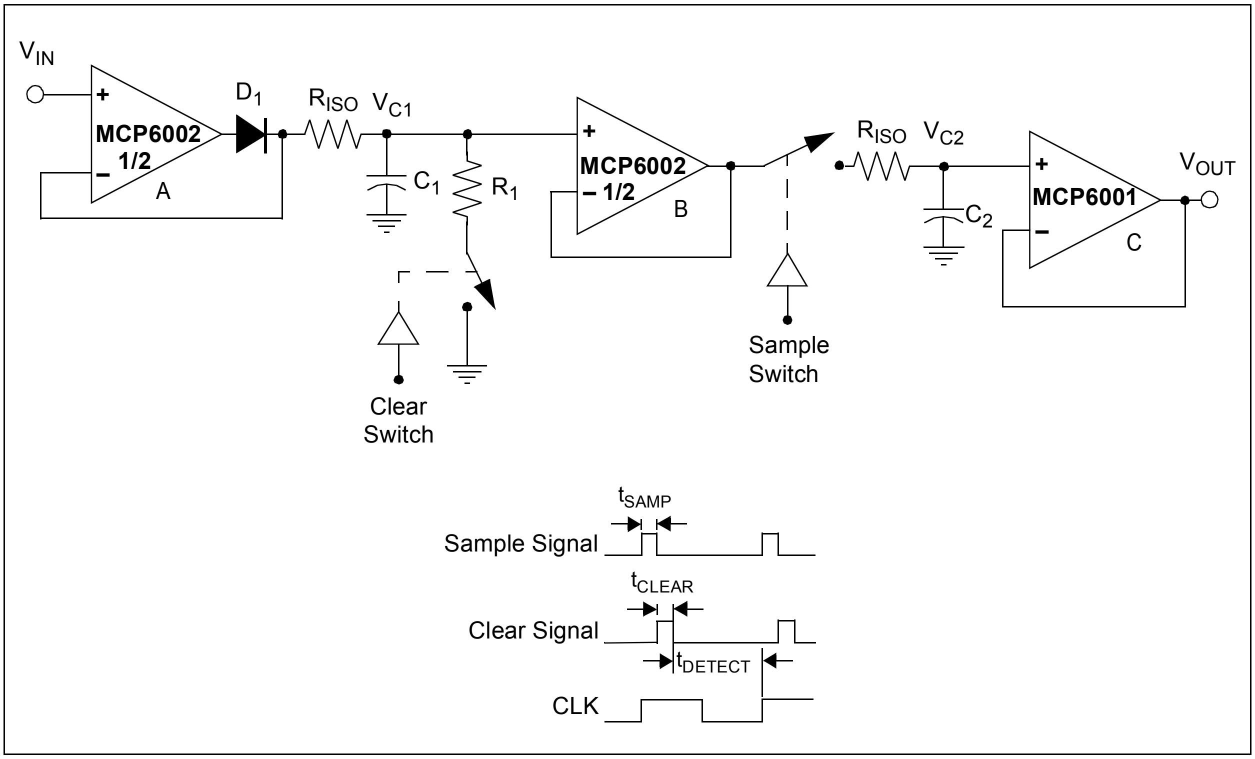



***FIGURE 3-7:*** *Peak Detector with Clear and Sample CMOS Analog Switches.*