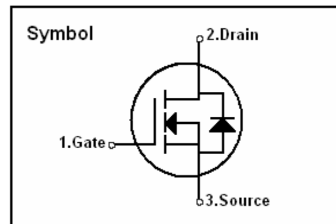
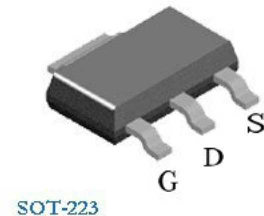
600V N-Channel MOSFET

Features

- 1.0A,600v,RDS(on)=9.3 Ω@VGS=10V
- Gate charge (Typical 7.0nC)
- High ruggedness
- Fast switching
- 100% AvalancheTested
- Improved dv/dt capability





General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe, DMOS technology.This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics, such as fast switching time,low on resistance.low gate charge and especially excellent avalanche characteristics.This power MOSFET is usually used at AC adaptors, on the battery charger and SMPS.

Absolute Maximum Ratings

Symbol	Parameter		HGP1N60S	Units
VDSS	Drain to Source Voltage		600	V
ID	Continuous Drain Current(@TC = 25°C)		1.0	A
	Continuous Drain Current(@TC = 100°C)		0.65	A
IDM	Drain Current Pulsed	(Note 1)	4.0	A
VGS	Gate to Source Voltage		±30	V
EAS	Single Pulsed Avalanche Energy	(Note 2)	52	mJ
EAR	Repetitive Avalanche Energy	(Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
PD	Total Power Dissipation(@TC = 25 °C)		30	W
	Derating Factor above 25 °C		0.23	W/ °C
TSTG, TJ	Operating Junction Temperature & Storage Temperature		-55 ~ 150	°C
TL	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	°C

Thermal Characteristics

Symbol	Parameter			
RθJC	Thermal Resistance, Junction-to-Case	4.2	4.2	°C/W
RθCS	Thermal Resistance, Case-to-Sink Typ	50	50	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	110	110	°C/W

Electrical Characteristics (TC = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	600	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature coefficient	I_D = 250uA, referenced to 25 °C	-	0.4	-	V/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 600V, V_{GS} = 0V	-	-	1	uA
		V_{DS} = 480V, T_C = 125 °C	-	-	10	uA
I_{GSS}	Gate-Source Leakage, Forward	V_{GS} = 30V, V_{DS} = 0V	-	-	100	nA
	Gate-source Leakage, Reverse	V_{GS} = -30V, V_{DS} = 0V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-state Resis-tance	V_{GS} =10 V, I_D = 0.5A -	-	-	10.23 (Note 4)	Ω
			-	-	9.30 (Note 6)	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} =0 V, V_{DS} =25V, f = 1MHz	-	174	340	pF
C_{oss}	Output Capacitance		-	185	370	
C_{rss}	Reverse Transfer Capacitance		-	80	160	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} =300V, I_D =1A, R_G =25Ω (Note 4, 5)	-	15	35	ns
t_r	Rise Time		-	75	140	
$t_{d(off)}$	Turn-off Delay Time		-	30	60	
t_f	Fall Time		-	35	60	
Q_g	Total Gate Charge	V_{DS} =480V, V_{GS} =10V, I_D =1.0A (Note 4, 5)	-	7.0	9	nC
Q_{gs}	Gate-Source Charge		-	1.0	-	
Q_{gd}	Gate-Drain Charge(Miller Charge)		-	3	-	

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Current	Integral Reverse p-n Junction	-	-	1.0	A
I_{SM}	Pulsed Source Current	Diode in the MOSFET	-	-	4.0	
V_{SD}	Diode Forward Voltage	I_S =1.0A, V_{GS} =0V	-	-	1.4	V
t_{rr}	Reverse Recovery Time		-	420	-	ns
Q_{rr}	Reverse Recovery Charge	I_S=1.0A, V_{GS}=0V, dI_F/dt=100A/us	-	0.42	-	uC

※ NOTES
1. Repeativity rating : pulse width limited by junction temperature
2. L =95mH, I_{AS} =1.0A, V_{DD} = 50V, R_G = 50Ω , Starting T_J = 25°C
3. I_{SD} ≤ 1.0A, di/dt ≤ 300A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially independent of operating temperature.
6. The F/T $R_{DS(ON)}$ is an estimated value for the bare die, actual results will depend on customer packaging materials and dimensions.

Fig 1. On-State Characteristics

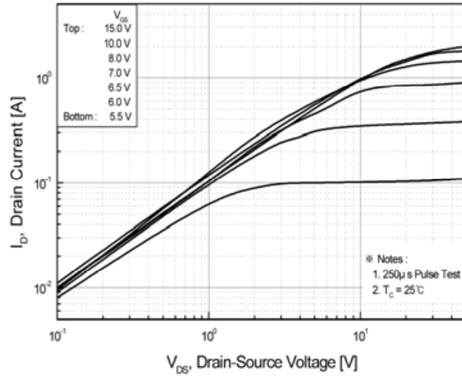


Fig 2. Transfer Characteristics

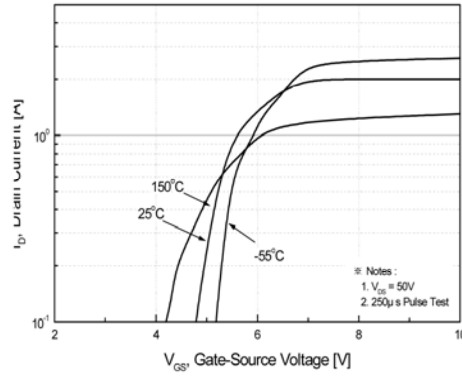


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

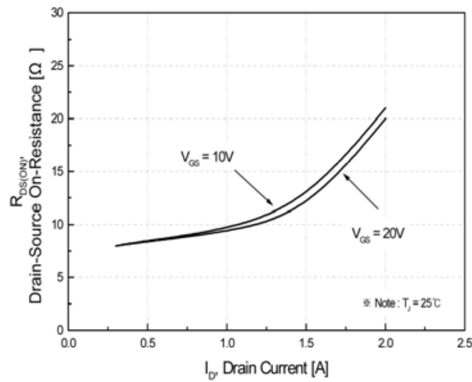


Fig 4. On State Current vs. Allowable Case Temperature

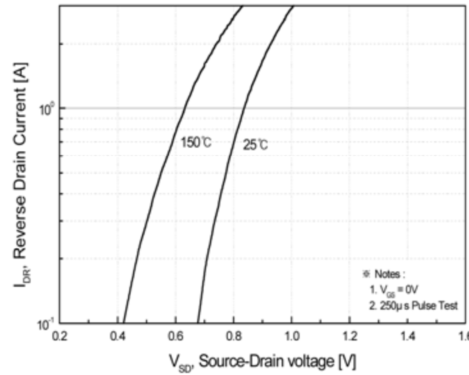


Fig 5. Capacitance Characteristics (Non-Repetitive)

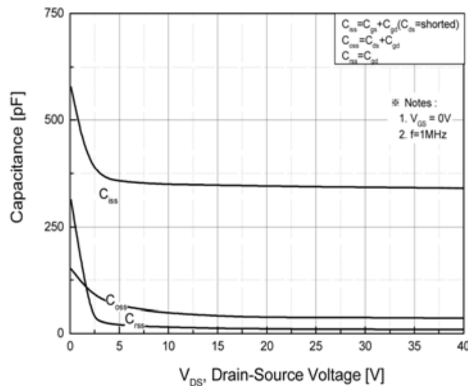


Fig 6. Gate Charge Characteristics

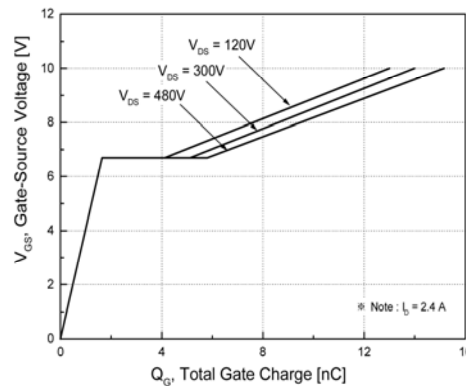


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

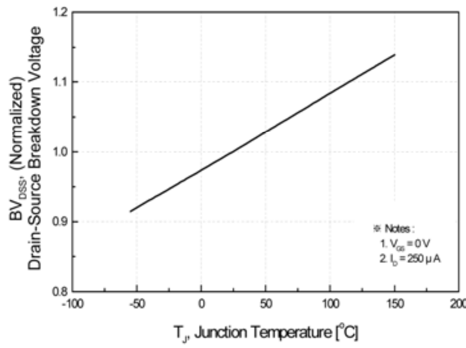


Fig 8. On-Resistance Variation vs. Junction Temperature

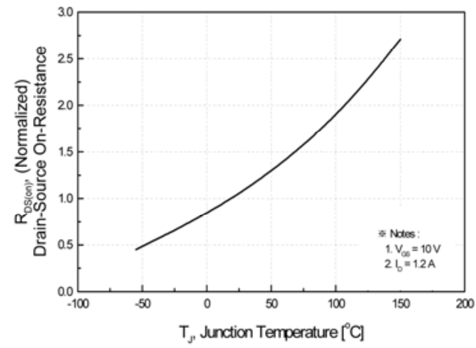


Fig 9-1. Maximum Safe Operating Area

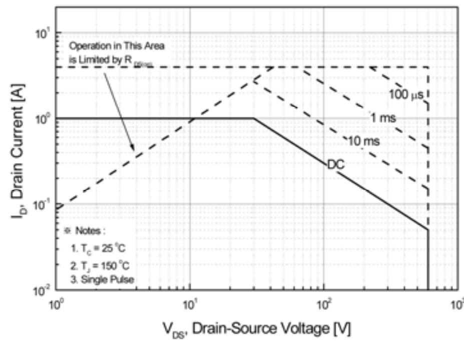


Fig 9-2. Maximum Safe Operating Area

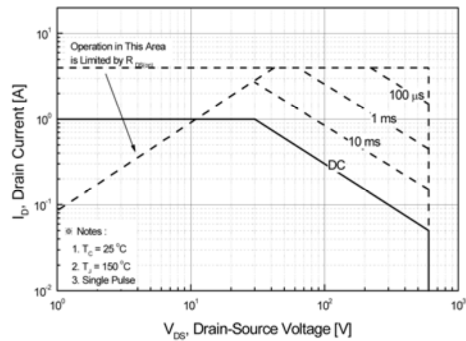


Fig 10. Maximum Drain Current vs. Case Temperature

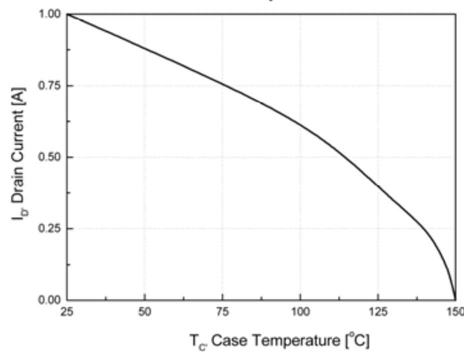


Fig 11-1. Transient Thermal Response Curve for TSD1N60

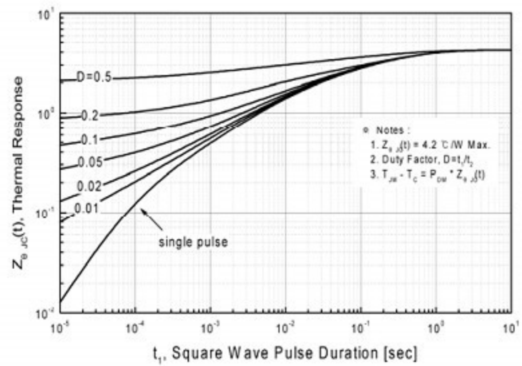


Fig. 12. Gate Charge Test Circuit & Waveforms

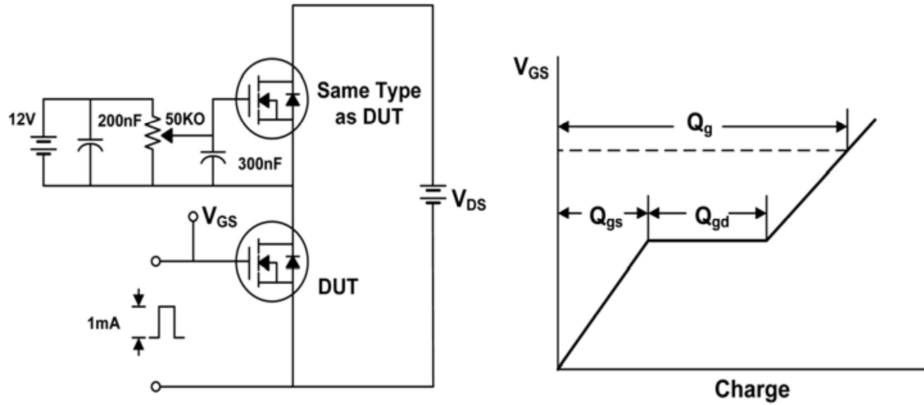


Fig 13. Switching Time Test Circuit & Waveforms

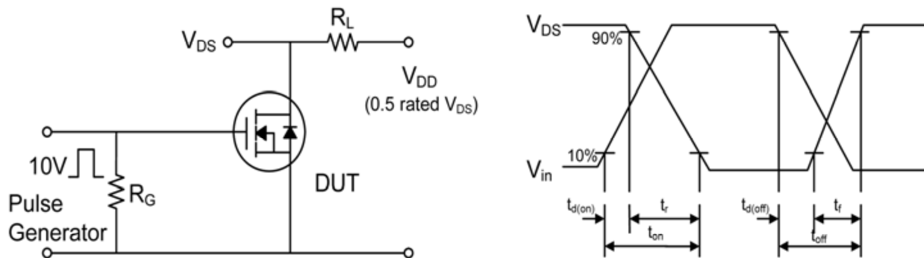


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

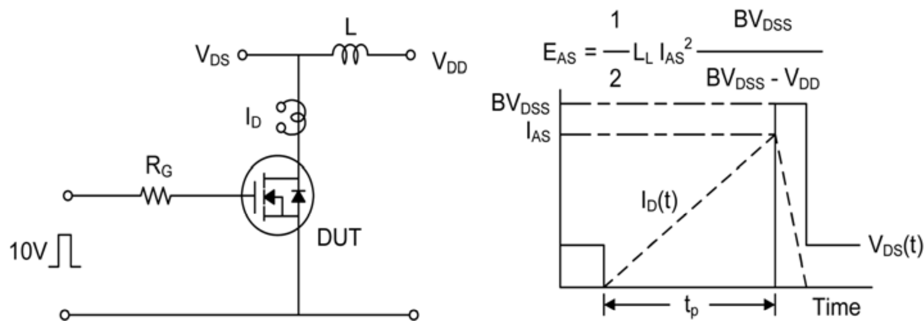


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms